

1. TECHNICAL DESCRIPTION

NOTE:

This technical description should be read in conjunction with the functional description given in Part 1, Chapter 4 of this manual.

Circuit diagram : Fig. 1.

1.1 Video Amplifier

All volt composite video signal is applied via SKT X1 pin 5 to the junction of R4 and C2. R4 acts as the terminating resistor for the connecting cable. Transistors V7, V12, V20, V25, V27, V30 form a video amplifier which ultimately drives the cathode of the CRT. Transistor V12 provides a buffered feed to the contrast control. The video amplifier up to V25 base is AC coupled, V20 provides DC clamping on the front porch of the video signal and from then on the amplifier is DC coupled. Line and frame blanking signals are applied via diodes V56 and V57 to the output stage V30. The output stage runs from a 60 volts stabilised supply with shunt peaking via L42 to improve the high frequency response and pulse rise-times.

1.2 Line Oscillator

This stage is built around TV horizontal processor IC D76. D76 combines the following functions:

- Horizontal sync. separation.
- Vertical sync. separation.
- Horizontal oscillator.
- Phase comparator.
- Composite blanking and key pulse generator.
- Output stage to line driver.

A positive composite sync signal is applied to D76-8 and -9 and pulses to drive the vertical output stages are obtained from D76-10. A horizontal output waveform is taken from D76-2 to drive the line output stage V100. The horizontal frequency is adjusted over a limited range by R84, this range being set by the networks C71, R73, R75, R72, C70 and C74. Feedback for the phase comparator is fed to D76-6 from the line output stage via R78.

1.3 Frame Oscillator and Output Stage

This stage is built around TV vertical deflection system IC D143. D143 performs the following functions:

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- Synchronisation circuit.
- Oscillator and ramp generator.
- High power amplifier.
- Flyback generator.
- Voltage stabilizer.

A frame sync pulse from pin 10 of horizontal processor 076 is fed to D143-8. A ramp output with sufficient current to drive the scan coil direct is taken from D143-4. Feedback from the output stage is provided by passing the output current through R127 applying the feedback voltage to D143-10 via R136. The output current and hence the frame scan amplitude is adjusted by varying the voltage fed back. Variable resistor R129 controls the height variation. Variable resistor R133 varies the oscillator frequency and R155 alters the feedback around the built-in ramp generator to provide a linearity adjustment.

1.4 Line Output and EHT Generator

V100 is the output driver for the line output stage. The circuit is conventional with the second harmonic tuning and energy recovery capacitor C106. Overwindings on the line output transformer T103 provide an EHT voltage of 8.5KV, a G2 voltage of 300 volts via V107 and C115 and a focus voltage of 0-300 volts via variable resistor R117.

Dynamic raster correction is provided by sampling the current flowing in the EHT lead and modulating the supply voltage to the output stage via V99. During the frame blanking period, signal is provided via R94 to stabilise the EHT output voltage.

The supply for the video stage and G1 is taken from pin 1 of the transformer T103 via V105 and R108 and then is stabilised by V47 before finally being smoothed by R45 and C43.

The brightness control R120 is taken from the +80 volts video supply and a -90 volt supply derived from flyback rectifying the same source. The range of brightness control is set by R121 and R119.

1.5 CRT Base Board

For flashover protection, CRT board assy 711 30650 0000 has spark gaps formed as part of the PCB tracking. R180, R182, R183 and R184 provide series current limiting. The CRT external conductive coating is grounded through the CRT base board via a flying lead to X185.

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2. FAULT FINDING

Typical operating waveforms and d.c. voltage levels have been added to the circuit diagram. Measurements were made with the user's brightness control pot. (CONTRAST) R14 set to maximum brightness. D.c. voltages were measured using a DVM (10 Megohm input impedance).

WARNING:

The VDD P8A generates a CRT electrode supply of 300V and an EHT of 8.5KV. These voltages are potentially lethal.

The CRT may remain charged at a high static potential for some time after the mains supply has been switched off. To avoid electric shock always earth EHT socket on CRT to discharge tube before handling. Do this before disconnecting EHT lead.

In the event of a blank screen, check that the CRT connector has not dropped off the end of the tube. The connector should normally be secured with a cable tie.

On the Secretarial Unit a blank screen will also occur if the logic cable is not properly connected, or if the associated Executive Unit is not switched on, or if 'Screen Blank' is selected.

If the display jitters when the user's brightness control is operated, change the pot.

Setting-up after repair is covered in Part 1, Chapter 7 of this manual.